UNIT-IV

(PROGRAMMABLE INTERFACING DEVICES)

8255A PPI-PROGRAMMABLE PERIPHERAL INTERFACING DEVICE

Introduction

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration. The 82C55A is fabricated on Intel's advanced CHMOS technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

Features

- It is Compatible with all Intel and Most Other Microprocessors
- It has High Speed, ``Zero Wait State'' Operation with 8 MHz 8086/88 and 80186/188
- Provides 24 Programmable I/O Pins
- Low Power CHMOS
- Completely TTL Compatible
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- 2.5 mA DC Drive Capability on all I/O Port Outputs
- It is available in 40-Pin DIP.
- Available in EXPRESS in Standard Temperature Range and also in Extended Temperature Range

Internal Architecture of 8255A:

- The parallel input-output (PIO) port chip 8255A is also called as programmable ***peripheral input-output port.*** The Intel's 8255A is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines.
- The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus Group A contains an 8-bit port A along with a 4-bit port C upper.
- The port A lines are identified by symbols PA0-PA7 while the port C lines are identified as PC4-PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0-PB7 and a 4-bit port C with lower bits PC0- PC3. The port C upper and port C lower can be used in combination as an 8-bit port C.
- Both the port C are assigned the same address. Thus one may have either three 8-bit I/O ports or two 8-bit and two 4-bit ports from 8255. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR).
- The internal block diagram and the pin configuration of 8255 are shown in fig below.
- The 8-bit data bus buffer is controlled by the read/write control logic. The read/write control logic manages all of the internal and external transfers of both data and control words. RD, WR, A1, A0 and RESET are the inputs provided by the microprocessor to the READ/ WRITE control logic of 8255.

The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus.

- This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.

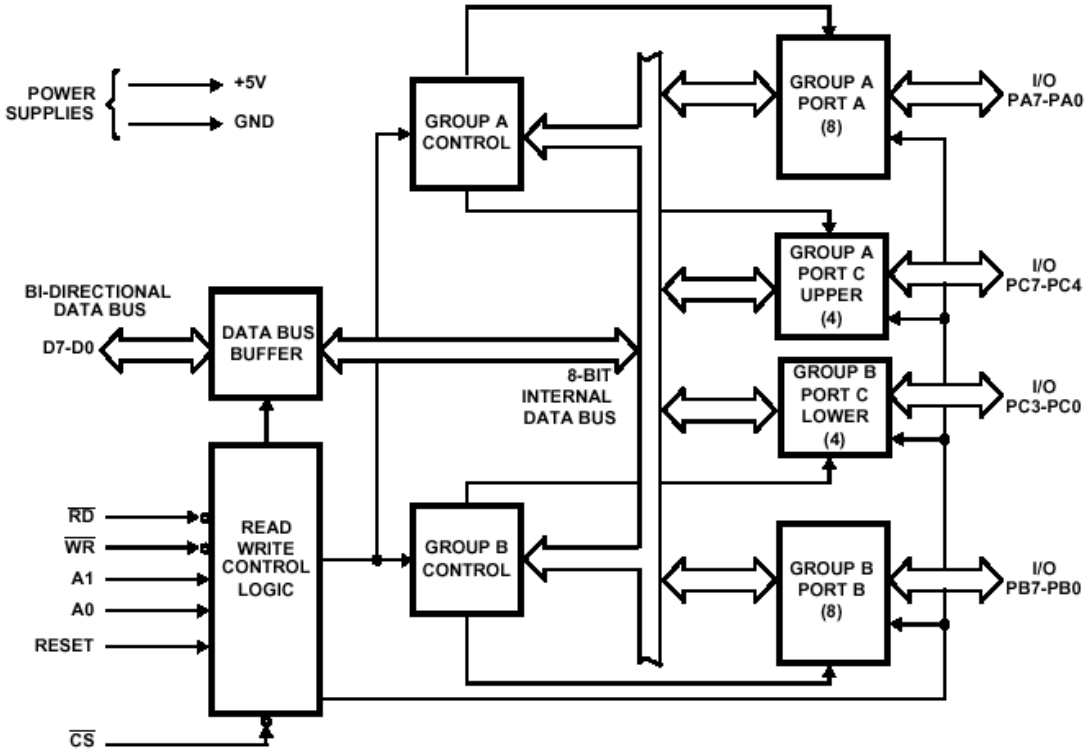


Fig. Internal Block diagram of 8255A PPI

Block Diagram Description:

The 8255A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the microprocessor. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the microprocessor Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the microprocessor ``outputs'' a control word to the 8255A. The control word contains information such as ``mode'', ``bit set'', ``bit reset'', etc., that initializes the functional configuration of the 8255A. Each of the Control blocks (Group A and Group B) accepts ``commands'' from the Read/Write Control Logic, receives ``control words'' from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7-C4)

Control Group B - Port B and Port C lower (C3-C0)

Ports A, B, and C

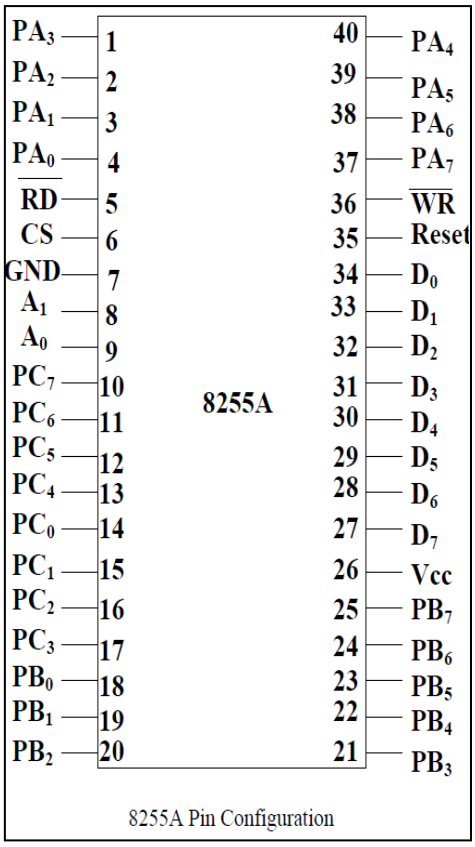
The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or ``personality'' to further enhance the power and flexibility of the 8255A.

Port A- One 8-bit data output latch/buffer and one 8-bit input latch buffer.

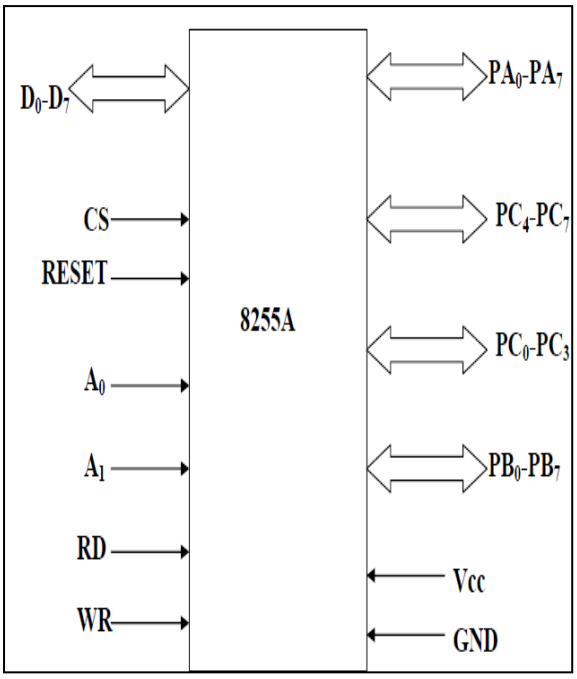
Port B- One 8-bit data input/output latch/buffer.

Port C-One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only

PIN DIAGRAM OF 8255A



8255A Pin Configuration



The signal descriptions of 8255 are briefly presented as follows:

- **PA7-PA0**: These are eight port A lines that acts as either output or input lines depending upon the control word loaded into the control word register.
- **PC7-PC4:** Upper nibble of port C lines. They may act as either output or input lines. This port also can be used for generation of handshake lines in mode 1 or mode 2.
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- **PC3-PC0:** These are the lower port C lines, other details are the same as PC7-PC4 lines.
- **PB0-PB7:** These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.
- $\overline{RD}$: This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.
- $\overline{WR}$: This is an input line driven by the microprocessor. A low on this line indicates write operation.

- $\overline{CS}$: This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.
- **A1-A0:** These are the address input lines and are driven by the microprocessor. These lines A1-A0 with RD, WR and CS form the following operations for 8255. These address lines are used for addressing any one of the four registers, i.e. three ports and a control word register as given in table below.
- In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the A0 and A1 pins of 8255 are connected with A1 and A2 respectively.
- **D0-D7:** These are the data bus lines those carry data or control word to/from the microprocessor.
- **RESET:** A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to Data bus
0	1	0	0	1	Port B to Data bus
0	1	0	1	0	Port C to Data bus
0	1	0	1	1	CWR to Data bus

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

MODES OF OPERATION OF 8255A PPI:

• These are two basic modes of operation of 8255.

1. Bit Set-Reset mode (BSR).
2. I/O mode

In BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.

In I/O mode, the 8255 ports work as programmable I/O ports. Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications.

a. Mode 0 (Basic I/O mode)
b. Mode 1 (Strobed input/output mode)
c. Mode 2 (Strobed bidirectional I/O***)***

All these modes can be selected by programming a register internal to 8255 known as CWR (Control Word Register) which has two formats. One is for BSR mode of operation and second one is for I/O mode of operation.

• ***BSR Mode***: In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to be set or reset is selected by bit select flags D3, D2 and D1 of the CWR as given in table.

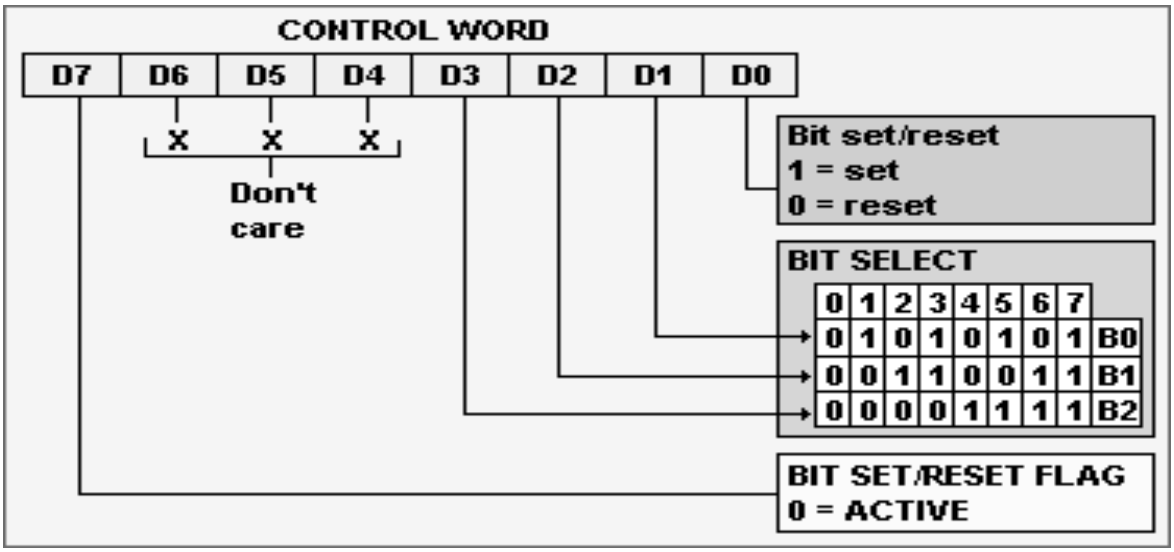

Fig. Control Word Register Format for BSR mode

• **I/O Modes:** The Control Word Register format for I/O mode of operation is shown below.

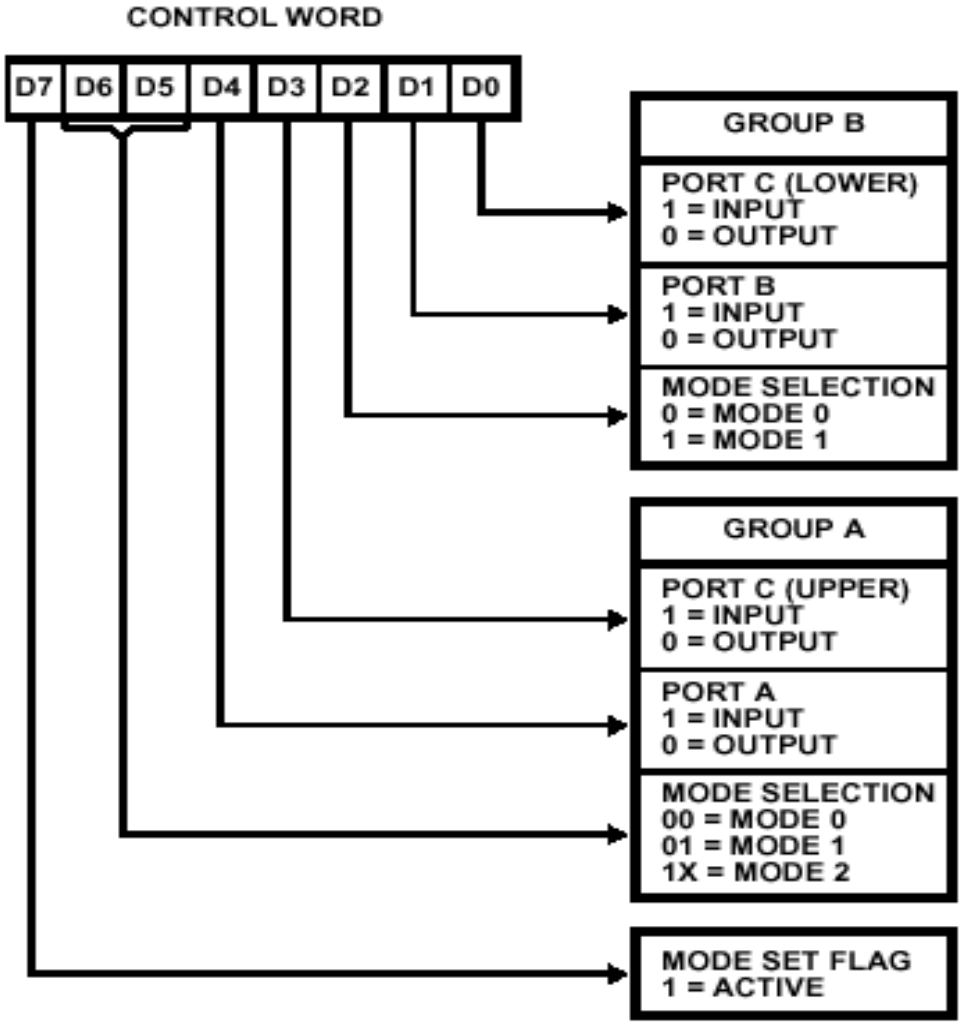

Fig. Control Word Register format for I/O mode operation

a) *Mode 0 (Basic I/O mode):* This mode is also called as *basic input/output mode*. When u want to use a port for simple input or output without handshaking, u initialize that port in mode 0.If both the port A and port B are initialized in mode 0, then the two halves of port C can be used together as an additional 8-bit

port, or they can be used individually as two 4-bit ports. When used as outputs, the port C lines can be individually set or reset by sending a special control word to the control register address. The two halves of port C are independent, so one half can be initialized as input, and the other half initialized as output.

b) Mode 1: ***(Strobed input/output mode):*** when you want to use port A or port B for a handshake (strobed) input or output operation, you initialize that port in mode 1. In this mode, some of ht epins of port C function as handshake lines. Pins PC0, PC1, and PC2 function as handshake lines for port B if it is initialized in mode 1. If port A is initialized as a handshake (mode 1) input port, then three pins PC3, PC4, and PC5 function as handshake signals. Pins PC6 and PC7 are available for use as input lines or output lines. If port A is initialized as a handshake output port, then port C pins PC3,PC6,and PC7 function as handshake signals. Port C pins PC4 and PC5 are available for use as input or output lines.

c). Mode 2 ***(Strobed bidirectional I/O):*** This mode of operation of 8255 is also called as strobed bidirectional I/O. This mode of operation provides 8255 with additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. Only port A can be initialized in mode 2. In mode 2, port A can be used for bidirectional handshake data transfer. This means that data can be output or input on the same eight lines. If port A is initialized in mode 2, then pins PC3 through PC7 are used as handshake lines for port A. The other three pins, PC0 through PC2, can be used for I/O if port be is in mode 0. The three pins will be used for port B handshake lines if port B is initialized in mode 1.

- **Interfacing 8255A with 8086:**

……..Refer Note book…….